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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,993	10/20/2003	Ok Byung Kim	0091.1030	1374

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EXAMINER	
GUHARAY, KARABI	

ART UNIT	PAPER NUMBER
2889	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/687,993	KIM ET AL.	
	Examiner	Art Unit	
	Karabi Guharay	2889	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE, filed on 11/12/2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7 and 11-13* is/are pending in the application.

4a) Of the above claim(s) *13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7,11 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/12/2008 has been entered.

Amendment, filed on 11/12/2008 has been considered and entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 5, 7 & 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Mitanaga et al. (US 5923997).

Regarding claims 1 & 11-12, Mitanaga discloses a display device (Active matrix LCD unit; lines 43-44 of column 7) with a polysilicon substrate (250; Fig 3b and 5a) comprising: a display region (pixel region) and a driving region (peripheral region containing driving circuits), a first plurality of TFTs in the display region (PTFT & NTFT);each transistor (see Fig 1C) including a source (111, 114 or 208 of Fig 3C), gate (107, 109; lines 39-44 of column 11) and drain (113, 116 or 210 of Fig 3C;lines 58 of column 11-line 32 of column 12); a second plurality of thin film transistors (PTFT & NTFT) in the driving region (lines 59-

50 of column 7 and lines 63 of column 9- line 4 of column 10) each transistor (see Fig 1C) including a source (111 or 114), gate (107, 109) and drain (113, 116); primary crystal grain boundaries (by definition; primary crystal grain boundaries are formed perpendicular to a crystal growth direction; so in case of Fig 5B primary crystal grain boundary is in direction perpendicular to direction of 215 or 216 of Fig 5B) in the polysilicon substrate in the display region and in the driving region, secondary crystal grain boundaries (secondary crystal grain boundary is formed in the same direction as the direction of crystal growth; in case of Fig 5B, direction of 215 is the direction of secondary crystal boundary) in the polysilicon substrate in the display region and in the driving region (though Mitanaga is silent about specific "primary" and "secondary" crystal grain boundary it is inherent that in crystallization process when crystals are growing, both primary grain boundary and secondary grain boundaries are formed perpendicular to each other); wherein the primary crystal grain boundaries are located within the gate regions of the first plurality of this TFT (with in the channel region 112, 115, or 209 of Fig 5A which is located in the gate region; see Fig 1C & 5A; lines 24-62 of column14) and are inclined to a first direction of current flowing from source to drain of each of the first plurality of TFTs in the display region at an angle of -30° to 30° (lines 31-40 of column 15; which teaches that in the pixel region crystal growth is perpendicular to the current flow direction, and since primary grain boundaries formed perpendicular to crystal growth direction so the primary grain boundaries in pixel region are parallel to the direction of current, thereby inclined at 0° angle); and the secondary crystal grain boundaries are located within the gate regions of the first plurality of this TFT (with in the channel region 112, 115, or 209 of Fig 5A which is located in the gate region; see Fig 1C & 5A; lines 24-62

of column14) and are inclined to a second direction of current flowing from source to drain (in this case direction of crystal growth is the direction of secondary crystal grain boundary direction) of each of the plurality of first plurality of TFTs in the display region;

and wherein the primary crystal grain boundaries are located with the gate regions of the second plurality of this film transistors and inclined to a second direction of current flowing from source to drain of each of the second plurality of thin film transistors in the driving region at an angle of 30°to 150° (lines 59 of column 7-lines 16 of column 8; in the driving region high mobility of carriers are required so the direction of crystal growth is same as the current direction, since primary grain direction is perpendicular to crystal growth direction; in case of peripheral TFTs in the driving region; primary crystal grain boundary is perpendicular to the current direction, would then be at an angle of 90°), while the secondary crystal grain boundaries are located within the gate of the second plurality of this TFT and are inclined at the first direction of the current flowing from source to drain of each of the second plurality of TFTs (though it is not disclosed explicitly, it is inherently inclined to 0 degree in this case, since secondary grain boundaries are always perpendicular to the primary grain boundary).

In regard to claim 2, Mitanaga et al ('997) teach the primary crystal grain boundaries of each of the first plurality of TFTs in the display region are parallel to the direction of current (lines 1-6 of column 8).

In regard to claim 5, the Applicant is claiming a display device including a method (i.e.: process) of making the polysilicon substrate; consequently, claim 5 is considered a "product-by-process" claim. In spite of the fact that a product-by-process claim may recite only process

limitations, it is the product and not the recited process that is coved by the claim. Further, patentability of a claim to a product does not rest merely on the difference in the method by which the product is made. Rather, it is the product itself, which must be new and not obvious (see MPEP 2113). Hence, Mitanaga et al's ('997) disclosure of a polysilicon substrate meets the structural limitation of the claimed invention.

In regard to claim 7, Mitanaga et al ('997) teach the primary crystal grain boundaries of each of the second plurality of transistors (TFTs used in the driving circuits in the periphery constituting the driving region) are perpendicular to the second direction of current (lines 6-16 of column 8).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mitanaga et al. (US 5923997).

In regard to claim 4, Mitanaga disclose all the limitations set forth, as described above, except the display device is an OLED. The Applicant, however, states that using TFTs in organic electroluminescent displays is known in the art in paragraph 9. The MPEP states that "[w]here

the specification identifies work done by another as "prior art," the subject matter so identified is treated as admitted prior art. In re Nomiya, 509 F.2d 566, 571,184 USPQ 607, 611 (CCPA 1975). Thus, it would have been obvious at the time of the invention to one of ordinary skill in the art to use the polysilicon substrate of Mitanaga as an OLED substrate. Motivation for combining would be to fabricate an active matrix OLED display.

Response to Arguments

Applicant's arguments filed 11/12/2008 have been fully considered but they are not persuasive. Response to applicant's arguments based on new limitations is provided in the rejection of amended claims above.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Karabi Guharay whose telephone number is 571-272-2452. The examiner can normally be reached on Monday-Friday 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minh-Toan Ton can be reached on 571-272-2303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Karabi Guharay/
Primary Examiner, Art Unit 2889